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In re: Gab-Jin Nam, *et al.*
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For: METHODS OF FORMING ELECTRONIC DEVICES INCLUDING DIELECTRIC LAYERS WITH DIFFERENT DENSITIES OF TITANIUM

Commissioner for Patents
Washington, D.C. 20231

**STATEMENT OF ACCURACY OF A TRANSLATION**
**37 CFR 1.52(d), 37 CFR 1.55(a) AND 37 CFR 1.69**

I, the below named translator, hereby state that:

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[ ] attached document
[X] below identified document,

Korean Application Serial No. 2002-0063024 as filed on October 16, 2002;

and I believe the attached English translation to be a true and complete translation of this document.

[X] This foreign language document was filed in the PTO on July 9, 2003.

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# SEMICONDUCTOR DEVICE HAVING DIELECTRIC LAYER IMPROVED IN TERMS OF DIELECTRIC CHARACTERISTICS AND LEAKAGE CURRENT AND METHOD FOR MANUFACTURING THE SEMICONDUCTOR DEVICE

## BACKGROUND OF THE INVENTION

This application claims priority from Korean Patent Application No. 2002-63024, filed 16 October 2002, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

1. Field of the Invention

The present invention relates to a semiconductor memory device and a method for manufacturing the semiconductor memory device, and more particularly, to a semiconductor memory device having a capacitor including a lower electrode, a dielectric layer, and an upper electrode and a method for manufacturing the semiconductor memory device.

2. Description of the Related Art

As the integration density of semiconductor memory devices increases, the area of a cell and the space between cells decrease. However, a capacitor has to maintain a prescribed capacitance, and thus the capacitor having high capacitance while occupying a small area is required. To ensure high capacitance in the capacitor, various measures have been suggested including using a high dielectric material as a dielectric layer, reducing the thickness of the dielectric layer, increasing the surface area of a lower electrode, and the like.

Among those suggestions, both the measures of increasing the thickness of the dielectric layer and increasing the surface area of the lower electrode have reached their limits, and thus the measure of increasing the capacitance by using a high dielectric layer is generally used.

A tantalum oxide ($Ta_2O_5$) film having a dielectric constant $\varepsilon$ of 24 is generally used for the dielectric layer of the capacitor.

Although a dielectric layer formed of the tantalum oxide film is advantageous in that the dielectric constant is high, it has following problems.

Firstly, the tantalum oxide film has an unstable chemical stoichiometric ratio thereby lacking oxygen, and thus leakage current is great. To replenish the film with oxygen, a thermal oxidation is applied to the tantalum oxide film.

However, during the thermal oxidation, the tantalum oxide film is easily penetrated by oxygen ions, and thus a silicon oxide film, which is generated by the upper electrode reacting with the oxygen ions, is formed at an interfacial surface between the tantalum oxide film and the lower electrode. Consequently, the thickness of an effective oxide of the dielectric layer (Toxeq) increases, and thus the dielectric constant of the tantalum oxide film decreases. Thus, the tantalum oxide film neither prevents a leakage current from occurring nor improves the dielectric characteristics.

## SUMMARY OF THE INVENTION

The present invention provides a semiconductor memory device having a dielectric layer improved in terms of dielectric characteristics and leakage current.

The present invention also provides a method for manufacturing the semiconductor memory device.

According to an aspect of the present invention, there is provided a semiconductor memory device comprising a semiconductor substrate, a lower electrode formed on the semiconductor substrate, a dielectric layer which is an oxide film including titanium and tantalum, on an upper surface of the lower electrode, and an upper electrode on an upper surface of the dielectric layer, wherein the density of titanium in the dielectric layer depends on the thickness of the dielectric layer.

The density of titanium of an area of the dielectric layer adjacent to the lower electrode is 0.1 to 15 percent.

According to another aspect of the present invention, there is provided a semiconductor memory device comprising a semiconductor substrate, a lower electrode formed on the semiconductor substrate, a reaction suppressing layer formed on an upper surface of the lower electrode, a first tantalum titanium oxide film formed on an upper surface of the reaction suppressing layer, a second tantalum titanium oxide film formed on an upper surface of the first tantalum titanium oxide film, and an upper electrode formed on an upper surface of the second tantalum titanium oxide film, wherein the density of titanium of the first tantalum titanium oxide film is 0.1 to 15 percent and the density of titanium of the second tantalum titanium oxide film is higher than or equal to the density of titanium of the first tantalum titanium oxide film. The

density of titanium of the second tantalum titanium oxide film is 0.001 to 3 percent. The density of titanium of the second tantalum titanium oxide film is 10 to 20 percent. The reaction suppressing layer is one of a silicon nitride film, a silicon oxide film, and a silicon oxynitride film. The lower electrode and the upper electrode are formed of at least one conductive film selected from a doped polysilicon film, a metal film, a metal oxide film, a metal nitride film, and a metal oxynitride.

According to another aspect of the present invention, there is provided claim a method for manufacturing a semiconductor memory device comprising (a) forming a lower electrode on an upper surface of a semiconductor substrate, (b) forming a dielectric layer of a oxide film including titanium and tantalum, on an upper surface of the lower electrode, and (c) forming an upper electrode on an upper surface of the dielectric layer, wherein, in step (b), the dielectric layer of a oxide film, the density of titanium in the dielectric layer depends on the thickness of the dielectric layer, and the density of titanium is adjusted to be 0.1 to 15 percent.

According to another aspect of the present invention, there is provided a method for manufacturing a semiconductor memory device comprising (a) forming a lower electrode on an upper surface of the semiconductor substrate, (b) forming a reaction suppressing layer on an upper surface of the lower electrode, (c) forming a first tantalum titanium oxide film on an upper surface of the reaction suppressing layer, (d) forming a second titanium oxide film on an upper surface of the first tantalum titanium oxide film, (e) applying a thermal process to the first and the second tantalum titanium oxide films under an oxygen atmosphere, and (f) forming an upper electrode on an upper surface of the second tantalum titanium oxide film, wherein a density of titanium is adjusted to be 0.1 to 15 percent when the first tantalum titanium oxide film is formed and a density of titanium of the second tantalum titanium oxide film is higher than or equal to the density of titanium of the first tantalum titanium oxide film. The density of titanium of the second tantalum titanium oxide film is 0.001 to 3 percent.

The reaction suppressing layer is formed by applying one of a rapid thermal nitridation, a rapid thermal oxidation, or a combination thereof to a surface of the lower electrode.

Steps (b) and (c) further comprises separately supplying a titanium precursor, a tantalum precursor, and oxygen gas into a reactor, and reacting the titanium precursor, the tantalum precursor, and the oxygen gas with each other within the reactor. The tantalum precursor is one of a metal alkoxide such as $Ta(OC_2H_5)_5$, an organometalic

such as a metal beta deketonate, and a metal halide such as $TaCl_5$. The titanium precursor is a compound such as one of $Ti(OCH(CH_3)_2)_4$, $Ti(OC_2H_5)_4$, $TiCl_4$, and a tetrakis-dimethylamido-titanium (TDMAT).

In steps (c) and (d), the tantalum precursor and the titanium precursor are mixed outside of the reactor and the mixed substance is supplied into the reactor. The tantalum precursor is pentaethoxy tantalum $Ta(OCH_2CH_3)_6$, (PET) and the titanium precursor is tetraethoxy titanium $Ti(OCH_2CH_3)_4$, (TET). A density of titanium in the dielectric layer is controlled by the deposition temperature and the flow rate of the precursor.

The tantalum titanium oxide film is formed under a temperature of 100 to 700℃ and a pressure of 100 to 760mTorr. In steps (c) and (d), the tantalum precursor and the titanium precursor are provided at a rate of 5 to 200mg/min and the oxygen gas is supplied at a rate of 10sccm to 10slm.

## BRIEF DESCRIPTION OF THE DRAWINGS

The above features and advantages of the present invention will become more apparent by describing in detail-preferred embodiments thereof with reference to the attached drawings in which:

FIG. 1 is a sectional view of a semiconductor memory device according to a first embodiment of the present invention;

FIGS. 2A through 2C are graphs showing density of titanium of a titanium tantalum oxide film with respect to the thickness of the titanium tantalum oxide film according to the first embodiment of the present invention;

FIG. 3 is a graph showing dielectric constant of a tantalum oxide film doped dopants;

FIG. 4 is a graph showing leakage current when a negative voltage is applied to a dielectric layer;

FIG. 5 is a schematic diagram of a first apparatus for depositing a dielectric layer according to the first embodiment;

FIG. 6 is a depiction of the chemical formula of a tantalum precursor and a titanium precursor which are used in a reactor external mixing method;

FIG. 7 is a graph for showing the TGA analysis result of a tantalum precursor, a titanium precursor, and a combination of the tantalum precursor and the titanium precursor;

FIG. 8 is a schematic diagram of a second apparatus for depositing a dielectric layer according to the first embodiment of the present invention;

FIG. 9 is a sectional view of a semiconductor memory device according to a second embodiment of the present invention;

FIG. 10 is a graph showing density of titanium with respect to the thickness of the tantalum titanium oxide film according to the second embodiment of the present invention;

FIG. 11 is a sectional view of a semiconductor memory device according to a third embodiment of the present invention; and

FIG. 12 is a graph showing density of titanium with respect to the thickness of the tantalum titanium oxide film according to the third embodiment of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

The present invention now will be described more fully with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete and will fully convey the concept of the invention to those skilled in the art. In the drawings, the thicknesses of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. It is also noted that like reference numerals may be used to designate identical or corresponding parts throughout the several views.

### First embodiment

Referring to FIG. 1, a silicon substrate, i.e., a semiconductor substrate 100, is provided. On a surface of the semiconductor substrate 100, a semiconductor device, a metal interconnection, and an insulating film may be formed. A lower electrode 110 is formed on an upper surface of the semiconductor substrate 100. The lower electrode 110 is formed of a doped polysilicon film, a metal film, a metal oxide film, a metal nitride film or a metal oxynitride film. In addition, the lower electrode 110 may be formed in a stack structure or have the shape of a box, a cylinder, a fin to a trench, or the like so as to increase its surface area.

On the surface of the lower electrode 110, a reaction suppressing layer 120 is formed. The reaction suppressing layer 120 is a layer for minimizing a reaction between the lower electrode 110 and a dielectric layer to be formed later. The reaction suppressing layer 120 may be formed of silicon nitride, silicon oxide, or silicon oxynitride, which may be treated by a rapid thermal nitridation (RTN), a rapid thermal oxidation (RTO), or a mixed treatment of RTN and RTO. The RTN can be performed at a temperature of 500 to 900℃ in an atmosphere including nitrogen, such as $NH_3$ or $N_2$. The RTO can be performed at a temperature of 500 to 900℃ in an atmosphere including oxygen, such as $O_2$ or $N_2O$. Here, it is possible to lower the activation energy by irradiating a plasma or ultraviolet ray, or the like, when performing the RTN, RTO, or the mixing treatment of RTN and RTO.

In addition, the reaction suppressing layer 120 may be formed by a chemical vapor deposition (CVD).

The reaction suppressing layer 120 suppresses a reaction between the surface of the lower electrode 110 and the dielectric layer, prevents oxygen ions from penetrating into the lower electrode 110 in cases of succeeding oxidation process and dispersion of an electric field applied to the dielectric layer. In the first embodiment, a silicon nitride film to which the RTN is applied is used for the reaction suppressing layer 120.

As the dielectric layer, a tantalum oxide film in which titanium is doped ($(Ta_2O_5)_{1-x}$ $(TiO_2)_x$:130, hereinafter referred to as a tantalum titanium oxide film 130) is deposited on an upper surface of the reaction suppressing layer 120. The tantalum titanium oxide film 130 is formed to have different densities of titanium according to its thickness. That is, the density of titanium of the tantalum titanium oxide film 130 may decrease as the thickness of the tantalum titanium oxide film 130 increases as shown in FIG. 2A, or the density of titanium of the tantalum titanium oxide film 130 may increase in proportion to the thickness of the tantalum titanium oxide film 130. Preferably, the density of titanium adjacent to the lower portion of the dielectric layer in the tantalum titanium oxide film 130 is about 0.1 to 15 % for the following reasons.

Referring to FIG. 3 which is a graph showing the dieletric contrast of a tantalum oxide film doped dopants, the tantalum oxide film is doped with titanium Ti, silicon Si, and zirconium Zr. The graph does not show great changes in the dielectric constant of the tantalum oxide film when the tantalum oxide film is doped with Si or Zr. However,

the dielectric constant of the tantalum oxide film is greatly improved when the tantalum oxide film is doped with titanium of 0.1 - 15 %, as shown in the graph.

Referring to FIG. 4 which is a graph showing leakage current when a negative voltage is applied to the dielectric layer, the effective oxide of the dielectric layer Toxeq and the leakage current are measured when the dielectric layer changes. Here, the dielectric constant increases as the thickness of the Toxeq decreases. In FIG. 4, ① denotes a case where a tantalum oxide film of a thickness of 70Å is formed, ② denotes a case where a tantalum titanium oxide film of a thickness of 50Å is deposited on the upper surface of the tantalum oxide film of a thickness of 20 Å, ③ denotes a case where a tantalum titanium oxide film of a thickness of 50Å is deposited on the upper surface of the tantalum titanium oxide film of a thickness of 20 Å, and ④ denotes a case where a tantalum titanium oxide film of a thickness of 70Å is formed. Here, the tantalum titanium oxide film includes titanium doped at 5~15 %.

According to the graph of FIG. 4, in case ①, the leakage current starts increasing when the thickness of the Toxeq is 31.8Å. In case ②, the leakage current starts increasing when the thickness of the Toxeq is 33.05Å. In case ③, the leakage current starts increasing when the thickness of the Toxeq is 31.9Å. In case ④, the leakage current starts increasing when the thickness of the Toxeq is 31.8Å.

As shown in the graph, the case where the tantalum titanium oxide film is deposited on the upper surface of the tantalum oxide film and the case where only the tantalum oxide film is formed are similar in terms of the thickness of the Toxeq at the starting point of the increase in the leakage current. In the case where the tantalum titanium oxide film is formed on the lower portion of the tantalum oxide film, the thickness of the Toxeq is not great as in the case where only the tantalum titanium oxide film is formed. That is, none of the dielectric layers using the tantalum titanium oxide film as a dielectric material have low dielectric constants; they can have optimal dielectric constants only when selected amount of titanium is included under a tantalum titanium oxide film.

Therefore, in this embodiment, the titanium is implanted into the tantalum oxide film as the dielectric substance, and the density of titanium at the interfacial area with the reaction suppressing layer 120 adjacent to the lower electrode 110 is adjusted to be 0.1 - 15%.

Here, the tantalum titanium oxide film 130 may be divided into two kinds of films according to how a precursor is supplied to the tantalum titanium oxide film.

Firstly, a tantalum precursor, a titanium precursor, and oxygen gas may be mixed within a reactor 200, e.g., a chamber. In this method, tantalum precursor, titanium precursor, and oxygen gas, which are changed into gas form, are separately supplied to a reactor 200. Here, they are supplied to the reactor 200 in gas form through a carrier gas such as hydrogen, helium, or nitrogen. The tantalum precursor, the titanium precursor, and the oxygen gas supplied into the reactor 200 are mixed within the reactor 200. The mixed gas in the reactor 200 reacts on the upper surface of the semiconductor substrate 100, preferably on the top surface of the reaction suppressing layer 120, and forming the tantalum titanium oxide film 130. Here, the density of titanium of the lower portion of the tantalum titanium oxide film 130 is adjusted to be 0.1 to 15 %. As shown in FIG. 5, an apparatus or equipments for performing the above process includes the reactor 200, a first reactant 210 which accommodates the tantalum precursor, a second reactant 220 which accommodates the titanium precursor, a third reactant 230 which accommodates oxygen gas, and gas lines 250a, 250b and 250c which connect the reactor 200 with the reactants 210, 220, and 230, respectively. Here, a metal alkoxide such as $Ta(OC_2H_5)_5$, an organometalic such as a metal beta deketonate, or a metal halide such as $TaCl_5$ may be used for the tantalum precursor. As the titanium precursor, compounds such as $Ti(OCH(CH_3)_2)_4$, $Ti(OC_2H_5)_4$, $TiCl_4$, or a tetrakis-dimethylamido-titanium (TDMAT) may be used. This method is advantageous in that the second reactant 220 accommodating the titanium precursor which supplies the titanium is separately formed, and thus the density of titanium can be easily controlled.

Secondly, the tantalum precursor and the titanium precursor may be mixed outside of the reactor, and then the mixed material may be supplied into the reactor.

As shown in FIG. 6, the tantalum precursor and the titanium precursor, in particular, a pentaethoxy tantalum Ta $(OCH_2CH_3)_6$ (hereinafter referred to as PET) and a tetraethoxy titanium $Ti(OCH_2CH_3)_4$ (hereinafter referred to as TET), are similar to each other in structure where a plurality of pentaethoxy groups ($OCH_2CH_3$) are connected to the one metal atom. Therefore, if the PET and the TET are mixed, the mixed precursor has some of the characteristics of the PET and some of the characteristics of the TET and moves as if it is one material.

Consequently, as shown in FIG. 8, first the PET precursor and the TET precursor are mixed in a reactant 240 outside of the reactor 200. Then the mixed precursor is supplied to the reactor 200, and the tantalum titanium oxide film 130 is

formed. Reference numeral 250d denotes a gas line which connects the reactant 240, including the mixed precursor, to the reactor 200.

Here, the density of titanium may be controlled by process conditions within the reactor 200. The process conditions include the deposition temperature, the deposition pressure, the flow rate of the precursor, the flow rate of the carrier gas, and the flow rate of oxygen gas, or the like. In particular, the deposition temperature and the flow rate of the precursor are closely connected with the density of titanium. That is, according to an experiment, if the deposition temperature increase 450℃ to 500℃, the density of titanium within the tantalum oxide film increases 1.7% - 4.2%. In addition, if the flow rate of the titanium precursor within the mixed precursor increases 16% - 50%, the density of titanium increases 17.6%. Thus, the density of titanium may be adjusted based on results from the experiment. This process is advantageous in that the structure of the reactor may be simplified.

The tantalum titanium oxide film 130 formed using the above processes is formed at a temperature of under 100 to 700℃, preferably, under 400 to 500℃, and at a pressure under 100 to 760mTorr. In addition, it is desirable for the tantalum precursor and the titanium precursor to be supplied at a rate of 5 to 200mg/min and for the oxygen gas to be supplied at a rate of 10sccm to 10slm when the tantalum titanium oxide film 130 is deposited.

Here, between the process of forming the reaction suppressing layer 120 and the process of depositing the tantalum titanium oxide film 130, a process of flowing a tantalum gas for more effective deposition may be included.

Returning to FIG. 1, the tantalum titanium oxide film 130 processed as described above is thermally processed so as to prevent leakage current. It is desirable to thermally process the tantalum titanium oxide film 130 under an oxygen atmosphere. Energy sources for the thermal process may be heat, ozone ($O_3$), oxygen plasma ($O_2$-plasma), or ultraviolet ozone (UV-$O_3$). Further, $O_2$, $O_3$, or $N_2O$ gas may be supplied into the reactor to create the oxygen atmosphere.

When the thermal process is performed, oxygen ions may penetrate into the tantalum titanium oxide film 130. However, the reaction suppressing layer 120 at the interfacial area of the lower electrode 110 and the tantalum titanium oxide film 130 prevents the oxygen ions from penetrating into the tantalum titanium oxide film 130 so that an undesired oxide film cannot be formed. Thus, the thickness of the Toxeq may

be reduced. In addition, the thermal process can be repeated in consideration of the leakage current.

Referring to FIG. 1, an upper electrode 140 is formed on the upper surface of the tantalum titanium oxide film 130. The upper electrode 140 may be a conductive layer such as a doped polysilicon film, a metal film, a metal oxide film, a metal oxynitride film, or the like. In this embodiment, TiN is used for the upper electrode 140. TiN has a low reactivity to the dielectric layer, and thus deterioration of the dielectric layer can be prevented.

According to this embodiment, a decrease in the dielectric constant can be prevented by using the tantalum titanium oxide film as the dielectric layer while the thermal process is performed for preventing the leakage current. Consequently, leakage current can be prevented, and the dielectric characteristics can be improved.

Second embodiment

FIG. 9 is a sectional view of a semiconductor memory device according to a second embodiment of the present invention, and FIG. 10 is a graph showing the density of titanium with respect to the thickness of the tantalum titanium oxide film according to the second embodiment of the present invention. In this embodiment, the same elements as those of the first embodiment will have the same reference numerals and overlapping descriptions will be omitted.

Referring to FIGS. 9 and 10, a first tantalum titanium oxide film 132, into which high-density titanium is doped, is deposited on the upper surface of the lower electrode 110 over the semiconductor substrate 100. The density of titanium (X2) of the first tantalum titanium oxide film 132 is about 0.1 to 15%, preferably, about 7.5 to 8.5%.

A second tantalum titanium oxide film 134, into which low-density titanium is doped, is deposited on the upper surface of the first tantalum titanium oxide film 132. The density of titanium (X1) of the second tantalum titanium oxide film 134 is lower than X2 and contains about 0.001 to 3% titanium.

In addition, the first and the second tantalum titanium oxide films 132 and 134 are formed by supplying the precursors separately or the mixed precursor to the reactor. Further, it is preferable that the first and the second tantalum titanium oxide films 132 and 134 be formed successively.

After that, the thermal process is performed, and the upper electrode 140 is formed in the same manner as the first embodiment.

As explained above, although the tantalum titanium oxide film is formed to be multilayered, the effects thereof are the same as in the first embodiment.

Third embodiment

FIG. 11 is a sectional view of a semiconductor memory device according to a third embodiment of the present invention and FIG. 12 is a graph showing the density of titanium with respect to the thickness of the tantalum titanium oxide film according to the third embodiment of the present invention. In this embodiment, the same elements as those of the first and the second embodiments will have the same reference numerals, and overlapping descriptions will be omitted.

Referring to FIGS. 11 and 12, a first tantalum titanium oxide film 136, into which low-density titanium is doped, is deposited on the upper surface of the lower electrode 110 over the semiconductor substrate 100. Here, the first tantalum titanium oxide film 136 includes about 0.1~15% titanium.

A second tantalum titanium oxide film 138, into which high-density titanium is implanted, is deposited on the upper surface of the first tantalum titanium oxide film 136. Here, the second tantalum titanium oxide film 138 has higher density titanium than the first tantalum titanium oxide film 136 and, preferably, includes about 10 to 20% titanium.

As described above, the first and the second tantalum titanium oxide films 136 and 138 are formed by supplying the precursors separately or the mixed precursor to the reactor. It is preferable that the first and the second tantalum titanium oxide films 136 and 138 are formed successively.

After that, the thermal process is performed and the upper electrode 140 is formed in the same manner as the first and the second embodiments.

As explained above, although the tantalum titanium oxide film is formed to be multilayered, the effect thereof is same as the first and the second embodiments.

As described above, by using a tantalum titanium oxide film as a dielectric layer of a capacitor, the dielectric layer is formed such that the tantalum titanium oxide film adjacent to the lower electrode has the most suitable density of titanium.

Consequently, the decrease in the dielectric constant can be prevented by using the tantalum titanium oxide film as the dielectric layer while the thermal process is performed for preventing the leakage current. Consequently, leakage current can be prevented, and the dielectric characteristics can be improved. As a result, capacitance is increased.

While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims and equivalents.

What is claimed is:

1. A semiconductor memory device comprising:

a semiconductor substrate;

a lower electrode formed on the semiconductor substrate;

a dielectric layer which is an oxide film including titanium and tantalum, on an upper surface of the lower electrode; and

an upper electrode on an upper surface of the dielectric layer,

wherein the density of titanium in the dielectric layer depends on the thickness of the dielectric layer.

2. The semiconductor memory device of claim 1, wherein the density of titanium of an area of the dielectric layer adjacent to the lower electrode is 0.1 to 15 percent.

3. The semiconductor memory device of claim 1, wherein a reaction suppressing layer is further interposed between the lower electrode and the dielectric layer so as to prevent a reaction between the lower electrode and the dielectric layer.

4. The semiconductor memory device of claim 3, wherein the reaction suppressing layer is one of a silicon nitride film, a silicon oxide film, and a silicon oxynitride film.

5. The semiconductor memory device of claim 1, wherein the lower electrode and the upper electrode are formed of at least one conductive film selected from a doped polysilicon film, a metal film, a metal oxide film, a metal nitride film, and a metal oxynitride.

6. A semiconductor memory device comprising:

a semiconductor substrate;

a lower electrode formed on the semiconductor substrate;

a reaction suppressing layer formed on an upper surface of the lower electrode;

a first tantalum titanium oxide film formed on an upper surface of the reaction suppressing layer;

a second tantalum titanium oxide film formed on an upper surface of the first tantalum titanium oxide film; and

an upper electrode formed on an upper surface of the second tantalum titanium oxide film,

wherein the density of titanium of the first tantalum titanium oxide film is 0.1 to 15 percent and the density of titanium of the second tantalum titanium oxide film is higher than or equal to the density of titanium of the first tantalum titanium oxide film.

7. The semiconductor memory device of claim 6, wherein the density of titanium of the second tantalum titanium oxide film is 0.001 to 3 percent.

8. The semiconductor memory device of claim 6, wherein the density of titanium of the second tantalum titanium oxide film is 10 to 20 percent.

9. The semiconductor memory device of claim 6, wherein the reaction suppressing layer is one of a silicon nitride film, a silicon oxide film, and a silicon oxynitride film.

10. The semiconductor memory device of claim 6, wherein the lower electrode and the upper electrode are formed of at least one conductive film selected from a doped polysilicon film, a metal film, a metal oxide film, a metal nitride film, and a metal oxynitride.

11. A method for manufacturing a semiconductor memory device, the method comprising:

(a) forming a lower electrode on an upper surface of a semiconductor substrate;

(b) forming a dielectric layer of a oxide film including titanium and tantalum, on an upper surface of the lower electrode; and

(c) forming an upper electrode on an upper surface of the dielectric layer,

wherein, in step (b), the density of titanium in the dielectric layer depends on the thickness of the dielectric layer.

12. The method of claim 11, wherein, in step (b), the density of titanium is adjusted to be 0.1 to 15 percent.

13. The method of claim 11, wherein the method further comprises forming a reaction suppressing layer for suppressing a reaction between the lower electrode and the dielectric layer, between steps (a) and (b).

14. The method of claim 13, wherein the reaction suppressing layer is one of a silicon nitride film, a silicon oxide film, and a silicon oxynitride film.

15. The method of claim 14, wherein the reaction suppressing layer is formed by applying one of a rapid thermal nitridation, a rapid thermal oxidation, and a combination thereof to a surface of the lower electrode.

16. The method of claim 14, wherein the reaction suppressing layer is formed by chemical vapor deposition.

17. The method of claim 11, wherein step (b) further comprises:

separately supplying a titanium precursor, a tantalum precursor, and oxygen gas into a reactor; and

reacting the titanium precursor, the tantalum precursor, and the oxygen gas with each other within the reactor.

18. The method of claim 17, wherein the tantalum precursor is one of a metal alkoxide such as $Ta(OC_2H_5)_5$, an organometalic such as a metal beta deketonate, and a metal halide such as $TaCl_5$.

19. The method of claim 17, wherein the titanium precursor is a compound such as one of $Ti(OCH(CH_3)_2)_4$, $Ti(OC_2H_5)_4$, $TiCl_4$, and a tetrakis-dimethylamido-titanium (TDMAT).

20. The method of claim 11, wherein, in step (b), the tantalum precursor and the titanium precursor are mixed outside of the reactor and the mixed substance is supplied into the reactor.

21. The method of claim 20, wherein the tantalum precursor is pentaethoxy tantalum $Ta(OCH_2CH_3)_6$, (PET) and the titanium precursor is tetraethoxy titanium $Ti(OCH_2CH_3)_4$, (TET).

22. The method of claim 20, wherein a density of titanium in the dielectric layer is controlled by the deposition temperature and the flow rate of the precursor.

23. The method of claim 20, wherein the dielectric layer is formed under a temperature of 100 to 700℃ and a pressure of 100 to 760mTorr.

24. The method of claim 23, wherein the tantalum precursor and the titanium precursor are provided at a rate of 5 to 200mg/min and the oxygen gas is supplied at a rate of 10sccm to 10slm.

25. The method of claim 11, wherein the method further comprises applying a thermal process to the dielectric layer under an oxygen atmosphere, between steps (b) and (c).

26. A method for manufacturing a semiconductor memory device, the method comprising:

(a) forming a lower electrode on an upper surface of the semiconductor substrate;

(b) forming a reaction suppressing layer on an upper surface of the lower electrode;

(c) forming a first tantalum titanium oxide film on an upper surface of the reaction suppressing layer;

(d) forming a second titanium oxide film on an upper surface of the first tantalum titanium oxide film;

(e) applying a thermal process to the first and the second tantalum titanium oxide films under an oxygen atmosphere; and

(f) forming an upper electrode on an upper surface of the second tantalum titanium oxide film,

wherein a density of titanium is adjusted to be 0.1 to 15 percent when the first tantalum titanium oxide film is formed and a density of titanium of the second tantalum

titanium oxide film is higher than or equal to the density of titanium of the first tantalum titanium oxide film.

27. The method of claim 26, wherein a density of titanium of the second tantalum titanium oxide film is 0.001 to 3 percent.

28. The method of claim 25, wherein a density of titanium of the second tantalum titanium oxide film is 10 to 20% percent.

29. The method of claim 26, wherein the reaction suppressing layer is one of a silicon nitride film, a silicon oxide film, and a silicon oxynitride film.

30. The method of claim 29, wherein the reaction suppressing layer is formed by applying one of a rapid thermal nitridation, a rapid thermal oxidation, or a combination thereof to a surface of the lower electrode.

31. The method of claim 29, wherein the reaction suppressing layer is formed by chemical vapor deposition.

32. The method of claim 26, wherein steps (c) and (d) further comprise:

separately supplying a titanium precursor, a tantalum precursor, and oxygen gas into a reactor; and

reacting the titanium precursor, the tantalum precursor, and the oxygen gas with each other within the reactor.

33. The method of claim 32, wherein the tantalum precursor is one of a metal alkoxide such as $Ta(OC_2H_5)_5$, an organometalic such as a metal beta deketonate, and a metal halide such as $TaCl_5$.

34. The method of claim 32, wherein the titanium precursor is a compound such as one of $Ti(OCH(CH_3)_2)_4$, $Ti(OC_2H_5)_4$, $TiCl_4$, and a tetrakis-dimethylamido-titanium (TDMAT).

35. The method of claim 26, wherein, in steps (c) and (d), the tantalum precursor and the titanium precursor are mixed outside of the reactor and the mixed substance is supplied into the reactor.

36. The method of claim 35, wherein the tantalum precursor is pentaethoxy tantalum $Ta(OCH_2CH_3)_6$, (PET) and the titanium precursor is tetraethoxy titanium $Ti(OCH_2CH_3)_4$, (TET).

37. The method of claim 35, wherein a density of titanium in the dielectric layer is controlled by the deposition temperature and the flow rate of the precursor.

38. The method of claim 35, wherein the tantalum titanium oxide film is formed under a temperature of 100 to 700℃ and a pressure of 100 to 760mTorr.

39. The method of claim 38, wherein, in steps (c) and (d), the tantalum precursor and the titanium precursor are provided at a rate of 5 to 200mg/min and the oxygen gas is supplied at a rate of 10sccm to 10slm.

## ABSTRACT OF THE DISCLOSURE

Provided are a semiconductor memory device improved in terms of dielectric constant and leakage current and a method for manufacturing the semiconductor memory device. The semiconductor memory device comprises a semiconductor substrate, a lower electrode which is formed on the semiconductor substrate, a dielectric layer which is a oxide film including titanium and tantalum on an upper surface of the lower electrode, and an upper electrode on an upper surface of the dielectric layer, in which the density of titanium in the dielectric layer depends on the thickness of the dielectric layer. The density of titanium of an area of the dielectric layer adjacent to the lower electrode is 0.1 to 15 percent.